Atty. Docket No.: 3175-Z

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Laung-Terng Wang et al
Serial No. 10/086,214 Examiner James C. Kerveros
Filed: March 27, 2002 Art Unit 2133
For: Method and Apparatus for Diagnosing Failures in an Integrated Circuit Using Design-for-Debug (DFD) Techniques

AMENDMENT AFTER FINAL

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed October 5, 2005, applicants respond as follows:

Claims 85 - 103 are pending in the application.

The rejection of claims 85-87, 89-93 and 99 under 35 U.S.C. 102(e) as being anticipated by Swamy (US 6,686,759) is respectfully traversed.

As made clear in the amendment filed June 24, 2005, the present invention is mainly for debugging or diagnosing two or more scan cores and the invention debugs or diagnoses "at-speed" delay faults, so each scan clock must comprise two system clock cycles, whereas to debug/diagnose stuck-type delay faults, each scan clock can comprise only one clock cycle. Thus, applicants' invention uses the term "selected fault type" that allows the DFD circuitry